REMARKS/ARGUMENTS

In the Office action dated January 6, 2005, the Examiner continued to: (1) allow claims 22 and 23; (2) indicate that claims 5, 7-10, 16 and 18-21 would be allowed if rewritten in independent form; and (3) reject all remaining claims (claims 1-4, 6, 11-15 and 17) as obvious over Tran (U.S. Pat. No. 5,752,259) in view of Drako et al. (U.S. Pat. No. 5,371,877). Based on the arguments below, Applicants believe all claims are in condition for allowance.

With regard to claim 1, Applicants previously argued that the art of record did not disclose a multi-bank branch prediction array. The Examiner had primarily used a patent to Tran (U.S. Pat. No. 5,875,324) for this limitation. The Examiner now seems satisfied that Tran '324 does not disclose the multi-bank branch prediction array as claimed. The Examiner, however, now uses another patent (U.S. Pat. No. 5,752,259) to the same inventor, Tran, as a reference that allegedly teaches the claimed branch prediction array. Applicants disagree with the Examiner's analysis and conclusion.

To be clear, claim 1 requires a "branch predictor" that includes a "multi-bank prediction array that is used for predictions for conditional branch instructions." Further, the claimed branch predictor includes "branch control logic" that "ensure[s] that two accesses to said prediction array in the same cycle do not conflict." As claimed, it is the conditional branch prediction array, not the instruction cache, for which it is ensured that multiple accesses do not conflict.

Tran '259 discloses a multi-way instruction cache. See Fig. 5 and col. 6, lines 19-36 ("Instruction cache 22 is organized into banks."). Tran's branch prediction unit 37, however, is not described as comprising multiple banks. The Examiner seems to gloss over this fatal deficiency of Tran by considering the combination of the instruction cache 22 and the branch prediction unit 37 to be the claimed "branch predictor" having a "multi-bank prediction array." See Office action, page 2. Applicants respectfully submit that is an unfair reading of Tran '259. Quite simply, the instruction cache 22 is NOT the branch prediction unit 37 nor is it even a part of the branch prediction unit. Drako is also deficient in this

regard. For at least this reason, claim 1 and all claims dependent therefrom are allowable over the art of record.

As for claim 12, the art of record does not teach or suggest a "multi-bank" branch prediction array or "bank control logic...to ensure that two branch prediction accesses to said prediction array in the same cycle do not conflict." Accordingly, claim 12 and dependent claims 13-21 are allowable at least for that reason.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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